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Quarterly Technical Progress Report
of the
Information Engineering Laboratory
for the period
May-July 1977

September 1977

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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Department of Computer Science
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

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1. Introduction

This report marks the reinstitution of the Quarterly Technical Progress Report of the Information Engineering Laboratory. The report is intended to keep interested persons informed about the progress being made on various research projects being carried out by the Information Engineering Laboratory of the Department of Computer Science. Each report will list those projects which have been completed, summarize progress on those projects which are currently active, and provide introductory remarks on new projects.

At the present time the primary source of funding for these projects is through the Office of Naval Research on Contract N00014-75-C-0982. Since this report includes both ONR funded research and research funded by other (or no) agencies, each section of the report is divided into a part pertaining to ONR funded research and a part pertaining to reserach supported by other funds. In the latter case, the source is specified.

The research is carried out by half-time graduate research assistants (graduate students) under the direction of one or more faculty members. The final documentation on a given project is usually in the form of the students thesis (MS or Ph.D.). These theses are published as technical reports on the projects. In some cases technical reports are issued which are not theses and in such cases, these will also be listed.

Much of the research is the result of a research proposal and in such cases a more detailed account of the proposed research can be found by consulting the relevant proposal. In other cases the research is a result of ideas originating with a student or staff member. In either case, an introductory description of the proposed research will appear when a new project is introduced into the report. Thereafter only a brief synopsis will be included.

W. J. Kubitz

2. Summary of Projects Completed During the Quarter

Several projects were completed during this quarter. They are listed below by project number and name along with the technical report number and the abstract. All reports are available directly from the Department of Computer Science, University of Illinois, Urbana, IL 61801, the Engineering Documentation Center, 208 Engineering Hall, University of Illinois, Urbana, IL 61801 and most reports are available from the IEEE Computer Society Repository.

2.1 ONR Funded Projects

OPTOBUNDLE (#61)

"OPTOBUNDLE - A Unique Fiber Optic Multiplier", Pitt, Poppelbaum and Xydes, Report #UIUCDCS-R-77-882.

Abstract

This paper describes the design and construction of failsoft single digit decimal multiplier that exhibits almost total immunity to electromagnetic interference. Bundles of glass fiber light-guides not only carry the numerical information but actually perform the multiplication as well. Nearly trivial hardware requirements make the device both reliable and inexpensive.

BURFT (#67)

"APPLICATION OF BURST PROCESSING TO THE SPECTRAL DECOMPOSITION OF SPEECH", Xydes, Christ, Report #UIUCDCS-R-77-870.

Abstract

The application of Burst Processing to the problem of spectral decomposition of speech is discussed. It is shown that such a representation provides a viable alternative to conventional speech analyzers. A specific Burst implementation is presented.

BURSTLOCK (#68)

"BURSTLOCK: A Digital Phase-Locked Loop Using BURST Techniques", Robinson, Michael, Report #UIUCDCS-R-77-872.

Abstract

BURSTLOCK is a digital phase-locked loop implemented using Burst Processing. It is used in a receiver of commercial broadcast signals. It is also shown that BURSTLOCK has some theoretical advantages over conventional phase-locked loops.

LOGITUNER (#69)

"Digital Filtering Using BURST Processing Techniques", Wells, David, Report #UIUCDCS-R-77-871.

Abstract

This paper covers the use of Burst Processing in digital filtering design. The analysis of Burst filters and their use in digital radios is discussed in detail. A digital radio is implemented as a demonstration of Burst filtering.

BURSTLOGIC (#70)

"BURSTLOGIC: DESIGN AND ANALYSIS OF LOGIC CIRCUITRY TO PERFORM ARITHMETIC ON DATA IN THE BURST FORMAT"
Tietz, Leon Clemens Report #UIUCDCS- R77-895

Abstract

A family of processors has been developed to perform arithmetic on data in the burst format. The common building block of these circuits is a simple finite state machine called the Perverted Adder (PA) which performs BURST addition. The interconnection of PAs in a tree formation with some additional circuitry produces a Burst Multiplier or adder. A PA CPU has been constructed to demonstrate these PA designs.

2.2 Non-ONR Funded Projects

Source of funding is given in brackets: [source].

MUMS (#75) [EE and CS Department].

"A Communications Unit for a Multi-Microprocessor Network"

Kujawinski, Gary, Report #UIUCDCS-R-77-880

Abstract

The Communications Unit is an interconnection scheme for Microprocessor systems, structured around a MUMS bus, to provide inter-processor interaction and resource sharing.

Data transmission between busses and the COM-UNIT is synchronous serial over 5 lines. The COM-UNIT, which is basically a microprocessor controlled serial crossbar, communicates with each bus through a TIE module, which appears as a DMA device to the local processor. For small systems, direct TIE to TIE connections can be made as dedicated datapaths.

3. Progress Report on Continuing Projects

3.1 ONR Funded Projects

WALSHSTORE (Project #78)

INTRODUCTION

The WALSHSTORE project is concerned with the investigation and the design of a fail-soft storage system for two-dimensional images. The goal is for the storage system to be able to sustain damage to some parts in it but to perform in an acceptable manner in spite of the damage, even if in a degraded form.

The fail-soft storage is done in the Walsh-Hadamard transform domain and all the processing is digital. The investigation includes a feasibility study on the use of Burst Processing in the various parts of the system.

PROJECT STATUS

The theoretical work has been completed and a first draft of the WALSHSTORE final report has been written.

The report of the results (UIUCDCS-R-77-878) will be available in the next quarter. It includes a discussion of the theory of orthogonal transforms and their application to fail-soft storage systems for large pictures, applications of BURST processing to such systems, a description of the WALSHSTORE mahine and a comparison of simulation results to the actual performance of the machine.

Ehud Bracha

PREDICTORBURST (Previously known as BALPARC, Project #81)

INTRODUCTION

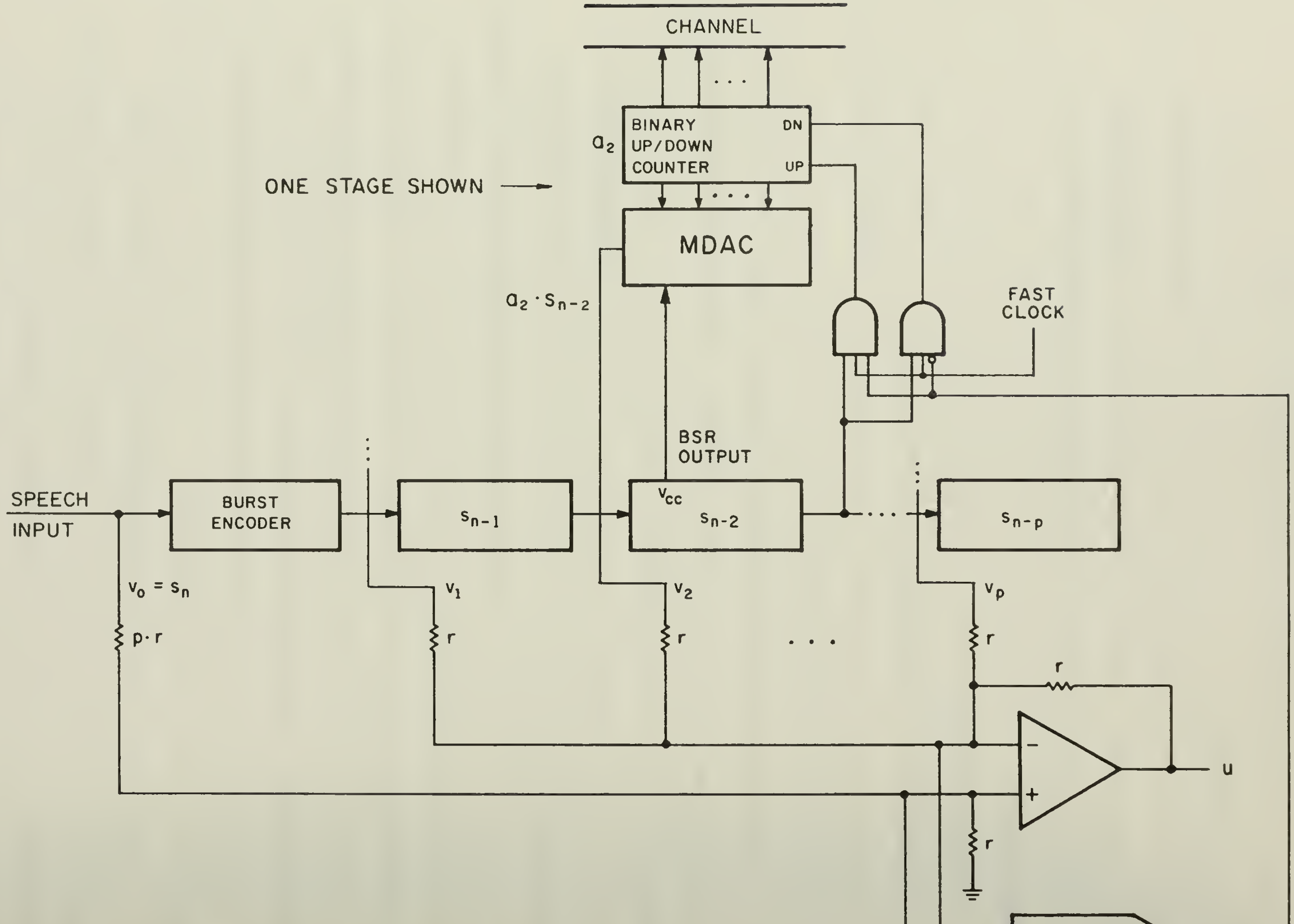
The goal of PREDICTORBURST is the on-line extraction of the predictor coefficients, needed in the linear predictive coding of speech, using BURST processing methods. The coefficients are then encrypted and transmitted by PCM.

PROJECT STATUS

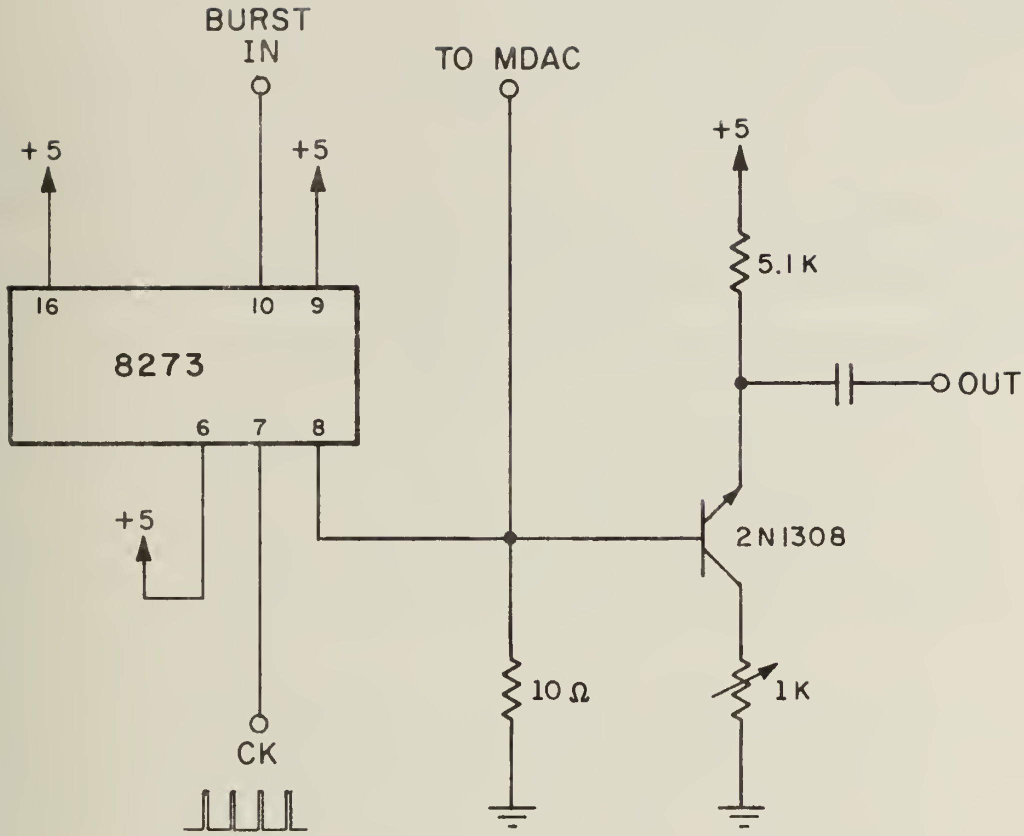
The design of this adaptive predictor, based on the least mean square gradient adaptive algorithm, has proceeded with progress in both the system and circuit design areas.

The system design problems with respect to coefficient precision and multiplication of past sample values by these coefficients have been remedied by the use of multiplying D/A converters (MDAC) as shown in Figure 3.1. The coefficient is represented by an 8-bit binary word in the up/down counter, and the previously used bidirectional shift register has been eliminated. This will provide more than sufficient precision for the coefficients as few designs in the literature specify more than 6 bits. Rather than effecting the multiplication by modulating the supply current of one register by the output current of another, a method which resulted in severe signal conditioning problems such as limited dynamic range, we form the product of the 8-bit coefficient word and the analog BSR output in one step by using the MC1408L8 MDAC.

The circuit design of the simplest BSR yet devised has been completed and is shown in Figure 3.2. Critical to this design are the use of the Signetics 8273 10-bit shift register, a Germanium, not Silicon transistor such as the 2N1308, and a clock with a duty cycle less than 2%. Staircase generators built with these components can produce up to eleven evenly spaced levels with virtually no ringing at the step transitions.



$$u = v_0 - \sum_{i=1}^{p} v_i = s_n - \sum_{i=1}^{p} a_i s_{n-i} \triangleq e_n$$



NOTE: UNNUMBERED PINS (PARALLEL OUTPUTS) NEED NO CONNECTION.

For Coefficient multiplication, the gain of the Germanium transistor is not needed, and the BSR output can be taken directly from pin 8 of the 8273 (retaining the 10Ω resistor of course) and connected directly to pin 14 of the MDAC through a 150Ω resistor.

Finally, the fast and slow clocks necessary for both the rapid level change required by the coefficients and the small duty cycle required by the BSRs have been designed, the frequencies being 3.11 MHz and 96.5 KHz respectively. This also allows the quantization of speech signals with frequencies up to 4500 Hz without aliasing.

Dan Pitt

MICROCARDALERT (Project #94) [EE and School of Clinical Medicine]

INTRODUCTION

"CARDALERT" is a microprocessor-based cardiac signal analyser. It detects the presence of premature ventricular contractions in heart beats due to heart diseases. By detecting these abnormal contractions, cardiac arrests can be predicted.

PROJECT STATUS

During the last quarter, the design of the system has been modified. Initially the memory locations for data storage were fixed so that the amount of hardware used in the system could be minimized in order to save space. However it was discovered that it was not flexible enough for program storage. Hence, in the modified version, several chips of D-latches and counters are included so that the starting location and the length of address can be specified separately by the program. This gives more flexibility to the program.

For this modified design initialization steps are needed to specify the starting address and the length of the address. This information is stored in two latches connected to the two counters. After each sampling of the data, a DMA request signal is generated by the A/D converter and, when the DMA grant signal is given out by the microprocessor, the data is stored in the memory location specified by the address location counter. The address location counter is then advanced by one and the address length counter decreased by one. When the address length becomes zero, the counters are reset to the values which are stored in the latches.

At present, the circuits for the modified version are completed and ready for testing and debugging. The designing and building of the data sampling part is also in progress.

Simon Lee

OTEMON (Project #95)

INTRODUCTION

A Continuous waveform visual monitor is being designed in the form of a small, cheap TV controller. It is primarily intended for the display of natural phenomena such as EKG signals, although other applications can be envisioned.

The controller divides the TV screen into a number of "bands" along which the signal is displayed. The number of bands is variable, and the resolution changes accordingly.

PROJECT STATUS

The initial design has been completed, achieving the goals described in the previous report.

All wiring diagrams and lists have been produced and a prototype is now under construction.

Some of the control circuitry, as well as the interface between the controller and the TV monitor, are currently operational. Completion of the memory, which is a fairly large shift register central to the design, awaits receipt of parts. A working prototype should exist within the next few months.

Carlos Mier

NETSURV (Project #84, previously nameless)

INTRODUCTION

This project is concerned with the design of a communication network of limited extend (a ship or building) which has properties such that its expected survivability is high even when it suffers multiple communication path loss.

PROJECT STATUS

Work on this project was suspended during the summer months and will be renewed next quarter.

3.2 Non-ONR Funded Projects

Source of funding is given in brackets: [Source]

Parallel Hardware Algorithms for High-Speed Function Generation (Previously known as HINA, Project No. 73). [DCS]

INTRODUCTION

We are considering the problem of high speed parallel hardware function generation. The function $f(x)$ is to be evaluated in the interval $[a,b]$. The interval $[a,b]$ is broken down into a few sub-intervals $\{x_i\}$ within which f is piecewise approximated by polynomials of the same degree. The coefficients of these polynomials are stored in ROMs. The argument x is not uniformly distributed since normalized floating point numbers have a logarithmic distribution. Using this fact our problem can be stated as follows:

> Minimize the <u>average</u> number of multiplications $M(X)$ necessary to evaluate [f(x) - (objective)] subject to a constraint on the number of ROM words $R_0(X)$ where X is the vector of sub-interval breakpoints $(x_0, x_1, \ldots x_m)$.

PROJECT STATUS

This is a non-linear programming problem (non-linear in both the objective and constraint function). There is no available program to solve a general NLP problem but there are programs to minimize a function of n variables. Because of this, the penalty function method for solving NLP problems was used. This method consists of replacing the problem

$$\begin{cases} \text{minimize } M(X) \\ \text{subject to } h(X) = R_0(X) - R_0 < 0 \end{cases} \quad (1)$$

by

$$\begin{cases} \text{minimize } \quad Q(X,\mu_n) = M(X) + \mu_n P(X) \\ \mu_n \to \infty \end{cases}$$

where P(X) in the penalty function obtained from h(X). For μ_n large enough the minimum of Q is a solution of (1).

In our case Q is not convex, but a grid search for starting values is avoided by taking into consideration the particular shape of Q.

We are now plotting the minimum average number of multiplications as a function of R_0 for the functions $1/x$, $\sqrt{x}$ and $\log x$.

Gilles Garcia

4. Progress Report on New Projects Begun this Quarter

This section introduces the five new projects begun during this quarter. In each case a more detailed description of the proposed work can be found in the proposal.

4.1 ONR Funded Projects

INDIRAD (Project #82)

INTRODUCTION

INDIRAD is a digital receiver for amplitude modulated radio signals which uses indicator representation (see below) for processing. The project consists of researching and developing methods of digital signal processing which are most naturally suited to indicator representation, and then applying these methods to design and build INDIRAD.

Indicator representation is basically decoded, weighted binary or a "one out of N" representation. Two indicator values can be used as row and column selection in a matrix, thereby allowing an arbitrary function of the two variables to be generated by "table lookup". This scheme is used to peak detect an AM radio signal as follows: Two samples, A and B, separated by one quarter period are taken each period of the carrier. Many A samples are averaged together to produce a D.C. level, and likewise for B. Note that sampling at the frequency of the carrier shifts the carrier frequency to D.C. The carrier peak can then be found by computing SQRT (A**2+B**2), which is easily accomplished using and indicator matrix.

PROJECT STATUS

During the past three months various digital signal processing methods have been studied. A versatile on-line computer simulation program was written which is providing a test ground for the filtering techniques developed.

The radio to be built will use 10,000 series ECL and standard TTL. It will receive AM stations from .5 to 100 MHz without heterodyning, and from 50 to 100 MHz without analog filtering. The exceptional speed of indicator processing makes the 10 ns addition times required in this radio possible.

Gary Gostin

BURFT II (Project #85)

INTRODUCTION

This project is an extension of the BURFT project (project #67, Report # UIUCDCS-R-77-870) and considers BURST implementation of more general transforms than the Fourier Transform. Thus, BURFT II will be a more general convolution machine which will implement the Karhunen-Loeve transform and the Hadamard transform in addition to the Fourier transform. This machine will use the same pitch detector circuit and the same type of clock circuit as was used in BURFT. However, sinusoidal analog signals used in BURFT will be implemented by means of a string of D/A converters fed from a ROM (read-only memory) in this enhanced version. This will allow each reference voltage being generated, and thus the entire output waveform to be changed rapidly. By changing the reference waveforms, it is possible to change the transform which is being implemented. The changes in the reference waveform may be made easily and quickly using either a microprocessor or hardwired logic thus facilitating selection of the desired transform.

PROJECT STATUS

The current effort is being devoted to finding a good, fast method for generating the harmonics necessary for computing the transforms other than the Fourier. After this decision is made, the hardware design will be completed and implementation will begin.

Norm Kelly

ILLIBOT (Project #86)

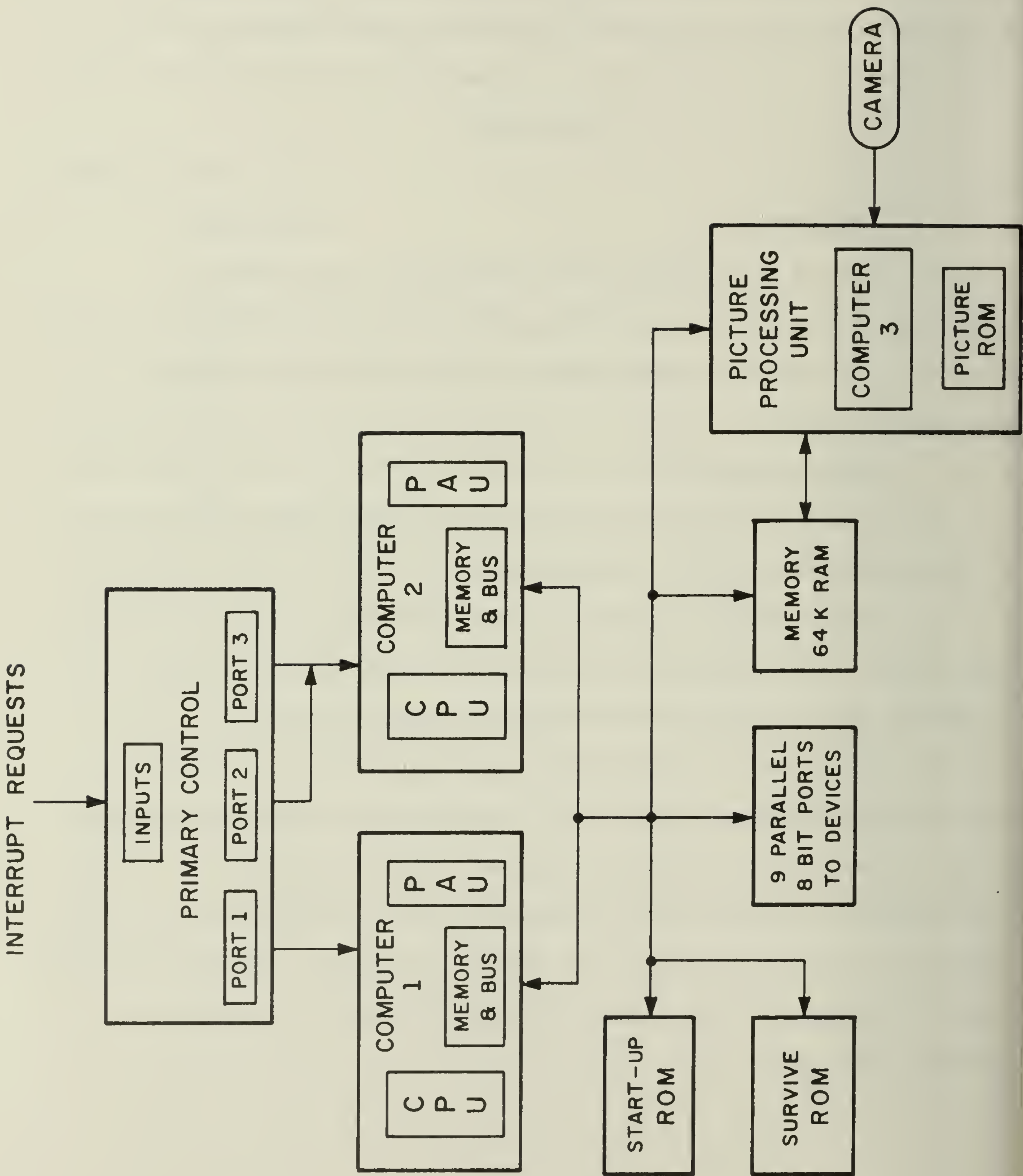
INTRODUCTION

The goal of this project is to construct a robot capable of surviving totally on its own in a potentially hostile environment. The robot will require no human guidance or interference under normal operating conditions.

THEORY OF ILLIBOT:

Illibot's purpose is to survive, obey commands and construct an understanding of the world, in that order.

Illibot operates through its primary control system (see Figure 3.3). This is essentially a sophisticated eight-input priority encoding interrupt subsystem that can mask and queue interrupt requests. This subsystem accepts inputs from both software and hardware and outputs to three ports. Port 1 is connected to the primary computer and ports 2 and 3 to the secondary computer. Port 3 is used only when Illibot is in survive mode. Otherwise, port 2 is connected to computer 2 so that both computers can operate concurrently. Each computer consists of a CPU, memory and bus controller, and a peripheral arithmetic unit (PAU).


INTERRUPT REQUESTS
INPUTS
PRIMARY CONTROL
PORT 1
PORT 2
PORT 3
COMPUTER 1
CPU
MEMORY & BUS
PAU
COMPUTER 2
CPU
MEMORY & BUS
PAU
START-UP ROM
SURVIVE ROM
9 PARALLEL 8 BIT PORTS TO DEVICES
MEMORY 64 K RAM
PICTURE PROCESSING UNIT
COMPUTER 3
PICTURE ROM
CAMERA

At power-up a one-shot resets all the subsystems of the robot. This triggers a second one-shot which instructs the processor to read from the start-up ROM which in turn instructs the processor to load the program from ROM into RAM. This operation, designated start-up, takes about 4 minutes. Upon completion, Illibot is ready to enter normal operation. Start-up will occur only after there has been a major hardware failure and repair aboard Illibot.

Under normal operation Illibot's computers service the first interrupt. If a higher priority interrupt occurs, either the computer will drop the current task and resume it after servicing the higher interrupt, or the computer will share time between the interrupt routines. In the latter case, the computer would give a larger percentage of its time to the higher priority.

The proposed arrangement of the priorities is as follows:

Highest	1.	Reversal of harm to humans and materials.
	2.	Surviving
	3.	Listening
	4.	Sight Control
	5.	Speaking
	6.	Moving
Lowest	7.	Environmental Changes

Interrupts will occur under the following circumstances: A level one if Illibot is in the process of, or is about to harm a human. The level one interrupts are caused by a software evaluation routine and by hardware feedback sensors. A level two occurs if a hardware interrupt indicates low battery, or if a software routine determines that Illibot is in immediate danger. A level 3 is generated by the speech

recognition computer (a future expansion.) after it recognizes a verbal command. This frees the main computer to operate as a monitor. A level 4 is generated by the picture recognition computer only after it takes a "snapshot" of the present scene and analyzes it for objects it (Illibot) can recognize. For example, by experimenting with stairs it synthesizes a mathematical representation of stairs. Utilizing the GENERAL program, the machine quickly learns to construct a model of its immediate environment so that it does not need to constantly service the level 4 interrupt. A level 5 is a software generated interrupt for the purpose of taking over the bus to output data to the speech synthesizer. Level 6 is almost identical to level 5 except that the output data goes to the motor registers. Level 7, the lowest proposed interrupt is usually software initiated. However, on occasion, limit switches may cause a hardware interrupt. The function of level 7 is to move data to a special set of motor registers.

In normal operation Illibot's computers service the interrupts in sequential-priority order. However, in SURVIVE mode Illibots hardware reorders the priorities described above to the following:

New Level	Old Level	
1	1	Reversal of Harm to humans and materials
2	2	Surviving
3	6	Moving
4	7	Environmental Changes
5	4	Sight Control
6	5	Speaking
7	3	Listening

This is done to facilitate fast movement to an outlet. In addition, Illibot conserves and monitors internal energy consumption and reorganizes its computing hardware architecture accordingly. Where previously computer one and computer two were operating in parallel, now computer two services all non-level-one interrupts and attempts to manuver Illibot to the nearest outlet. Computer two is permitted to violate level one interrupts. Simultaneously, computer one monitors all major functions of Illibot and "spoon feeds" computer two data that it might have otherwise spent time computing. Computer one services all level one interrupts immediately, determines if and how computer two caused it, and then modifies computer two's command.

Illibot is a theoretical machine. The basis of its operating theory is that it is an unrestricted device, meaning that it is free to explore and do as it wishes until it receives instructions. This type of Artificial Intelligence programming I believe is the only practical way to deal with the real world since there are so many variables.

In the near future, if a simulation of Illibot's hardware determines that the machine holds a promise, then Illibot will be constructed. At that point, it will be built on a modular basis; proving the operation of each module before starting the next.

PROJECT STATUS

The various motor timing circuits, control circuits, feedback circuits and sequencers have been tested in a small-scale robot designated ALPHA. ALPHA is entirely dependent upon a human for proper operation. This means that it is necessary to place metal strips (1" long by 1/4" wide) every ten feet on the floor to guide the robot.

ALPHA is also dependent upon a hardwired layout of the area in which it is to operate. Any error such as missing a foil sensor, running into a door, or a request to go into the room it is in, results in an audible alarm which must be reset by the human operator.

Jeff Glickman

XENOCOMM (Project #87)

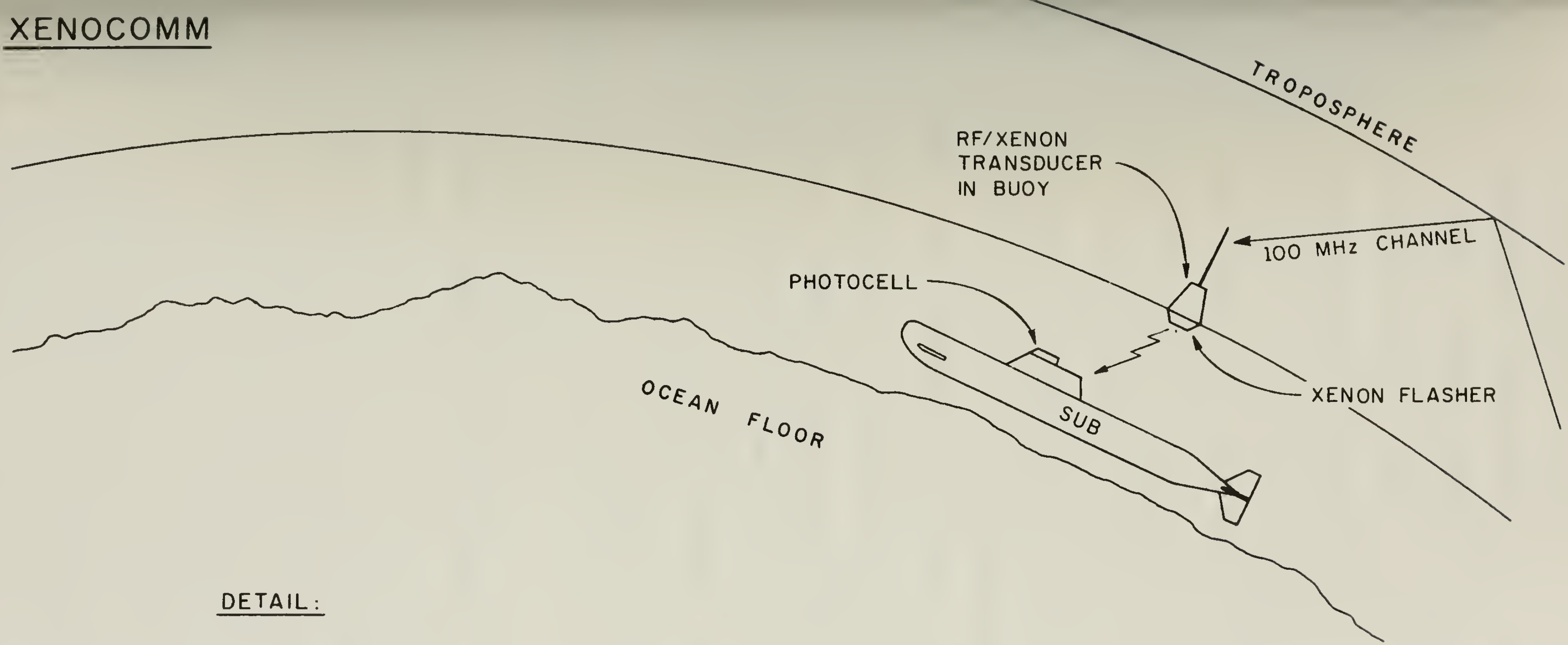
INTRODUCTION

The XENOCOMM project is an attempt to develop a system making possible communication to submarines while the submarines are submerged to depths of up to 1000 feet.

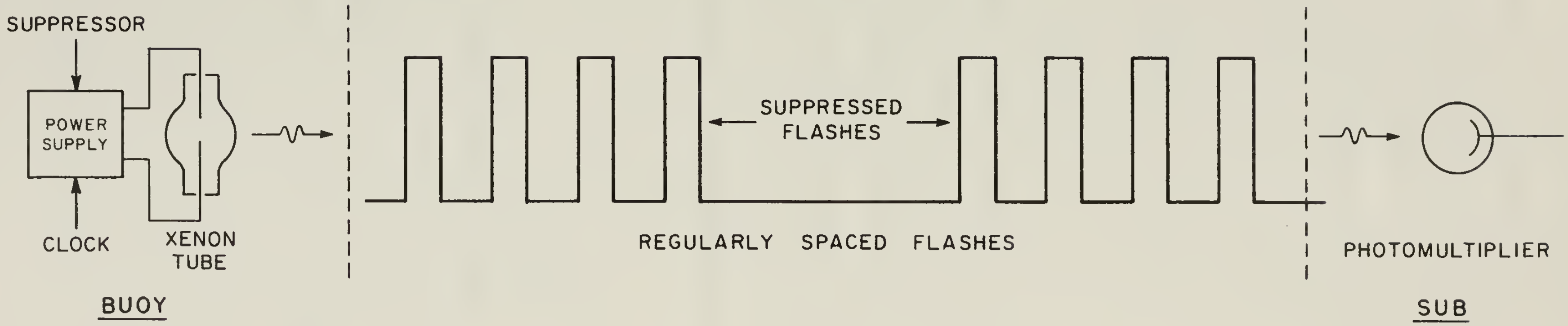
The initial proposal for XENOCOMM is as follows: A submarine will carry a large number (say 2000) of small, inexpensive buoys. Each will contain a radio for communication with ships, planes, land-based stations, etc. (A suitable frequency for these radios can probably be found in the 100 Mhz band.) Each time communication is desired the submarine will release a buoy. Communications between the submarine and the buoy will take place via a pulsed-light communication system.

The initial idea to be investigated is that of using a Xenon flashtube pulsing at 10,000 flashes per second. Certain flashes would be suppressed as a function of the audio signal demodulated from the radio receiver. The signal would probably be coded into BURST format for transmission over the pulsed-light system. A photomultiplier tube would be used as a receptor, and, if BURST encoding were used, the signal from this tube could be written directly into a BSR (Block Sum Register) for demodulation. This would result in an extremely simple communication system with the high noise immunity that results from BURST encoding. This system would be self-clocking and would have no need for synchronization. Figure 3.4 shows this system in symbolic form.

XENOCOMM



DETAIL:



BY MANIPULATING A SUPPRESSOR IN A POWER SUPPLY PRODUCING PERIODIC FLASHES, INFORMATION (e.g. VOICE) IS ENCODED IN BURST FORMAT. UPON RECEPTION, A BSR EXTRACTS THE MODULATION.

PROJECT STATUS

Since this project is new only initial studies have taken place so far. Attempts are being made to discover whether suitable light sources are available at reasonable costs. Studies are being made of the known properties of sea water in order to determine the required light output in the final working version. The construction of a circuit to experiment with various pulse rates and various BSR lengths (to determine the combination of pulse rate--BSR length which gives the best performance at suitable pulse rates) has begun.

At this point XENOCOMM appears to be feasible. If problems develop later, there are many alternatives that can be considered for most portions of the systems, e.g., other types of light sources could be considered (lasers, for example), other types of coding could be considered (although this would probably add to the complexity of the system), and other flash rates could be considered (provided light sources capable of performing at these rates can be found).

Randy Moss

PLANOBURST (Project #88)

INTRODUCTION

PLANOBURST uses Burst unary processors to implement a class of matrix processing functions characterized by two main features: first, the operation performed on a particular element is solely a function of the elements in a small surrounding neighbourhood, and second, the operation is to be repeated a number of times. A number of useful problems fall into this class, for example:

- correcting various deficiencies in a picture through gap-filling or edge detection.

- enhancement of an image, such as broadening or extending lines.
- the inverse of the previous operation; reducing a picture to a selected form.
- achieving bandwidth reduction for picture transmission by encoding the picture, transmitting it, and decoding the received version.
- simulation of the growth and decay of simple biological organizations.
- simulation of military strategy.

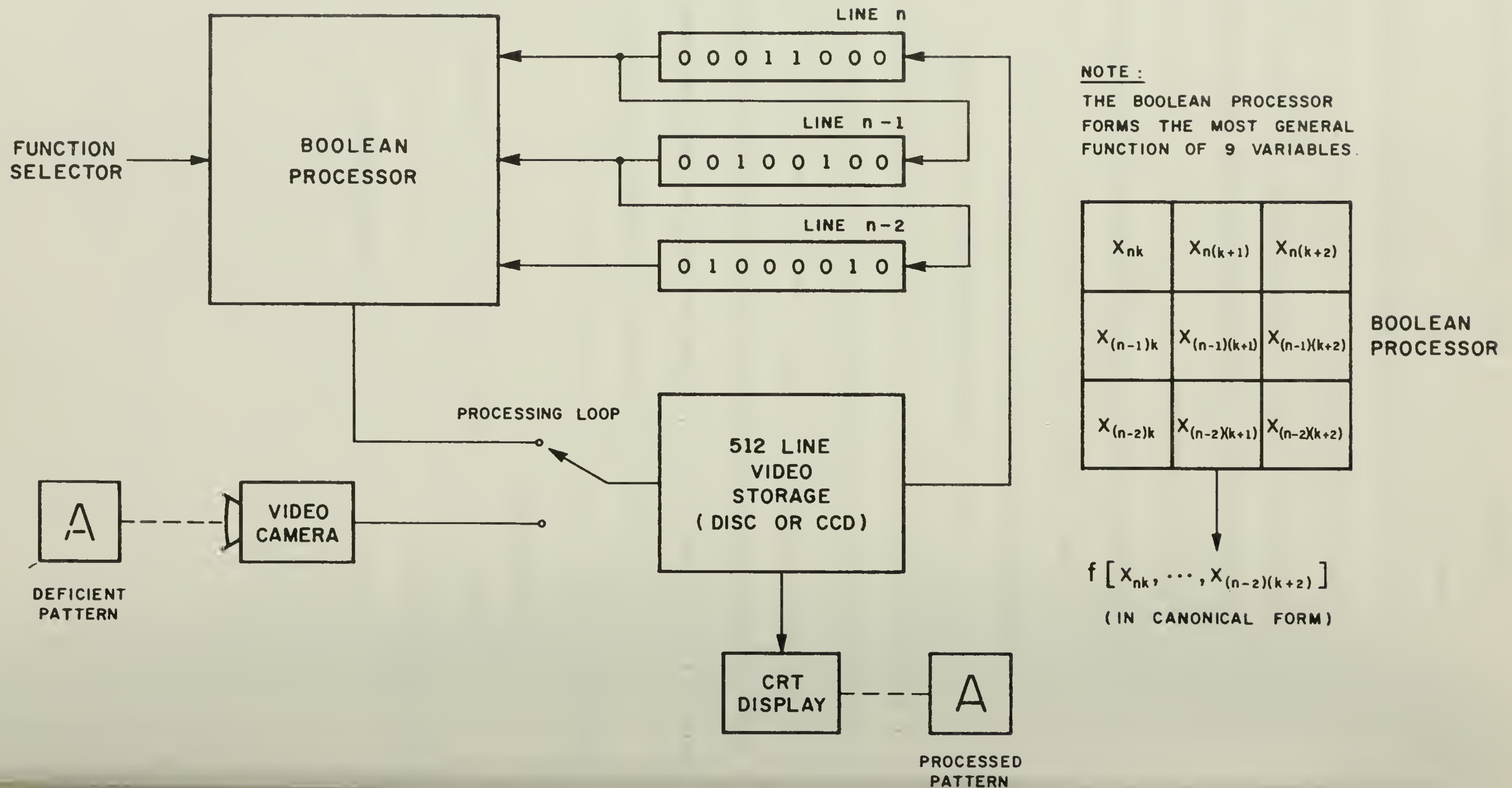
Figure 3.5 shows how PLANOBURST would implement simple processing of a 512x512 binary picture. The matrix circulates through a processor which examines only a 3x3 neighbourhood. The output of the processor flows back into storage to make up the next version of the matrix. When a sufficient number of iterations have occurred to produce an acceptable result, the processing loop is broken and the desired output is obtained.

It is obvious that there is a tradeoff between design complexity and the scope of the application area.

PROJECT STATUS

This project is new and all work has been devoted to its conceptualization.

Michael Robinson


FUNCTION SELECTOR
BOOLEAN PROCESSOR
LINE n
0 0 0 1 1 0 0 0
LINE n - 1
0 0 1 0 0 1 0 0
LINE n - 2
0 1 0 0 0 0 1 0
PROCESSING LOOP
512 LINE VIDEO STORAGE (DISC OR CCD)
A
DEFICIENT PATTERN
VIDEO CAMERA
CRT DISPLAY
A
PROCESSED PATTERN
NOTE:
THE BOOLEAN PROCESSOR FORMS THE MOST GENERAL FUNCTION OF 9 VARIABLES.
X_{nk} $X_{n(k+1)}$ $X_{n(k+2)}$
$X_{(n-1)k}$ $X_{(n-1)(k+1)}$ $X_{(n-1)(k+2)}$
$X_{(n-2)k}$ $X_{(n-2)(k+1)}$ $X_{(n-2)(k+2)}$
BOOLEAN PROCESSOR
$f\left[X_{nk}, \cdots, X_{(n-2)(k+2)}\right]$
(IN CANONICAL FORM)

4.2 Non-ONR Funded Projects

Source of funds is given in brackets: [source]

No new projects begun this summer.

5. References

For an explanation of BURST Processing see:

Poppelbaum, Wolfgang J., "Statistical Processors", Advances in Computers, Vol. 14, pp. 188-230.

For a summary of previous work please refer to the Annual Report issued by the Department of Computer Science.

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

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SUPPLEMENTARY NOTES

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Technical Progress Report
Computer Research Progress Report

ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report represents the abstracts for reports on recently completed research projects, summary statements on the status of current projects, and explanations of new projects at the Information Engineering Laboratory of the Department of Computer Science at the University of Illinois at Urbana-Champaign.

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lem ntary Notes

racts

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